REMARKS

At the outset, the Applicants appreciate the thorough review and consideration of the subject application. The Final Office Action of July 31, 2009 has been received and its contents carefully noted. By this amendment, claims 1, 41, and 48 have been amended. Claims 1, 3-7, 29, 30, 32-34, 41, 44-48 and 50-56 are currently pending. Support for these amendments are provided in at least the Figures and related text of the specification. No new matter has been added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Entry of this Amendment is respectfully requested because it places the present application in condition for allowance, or in the alternative, better form for appeal. In view of the above Amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Rejections Under 35 U.S.C. § 103

Claims 1, 3-7, 29, 30, 32-34, 41, 44-48, and 50-56 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent Application Publication No. 2004/0088469 A1 issued to Levy, U.S. Patent No. 6,295,566 issued to Stufflebeam and U.S. Patent No. 5,546,530 issued to Grimaud, *et al.* ("Grimaud"). Applicant respectfully traverses this rejection for at least the following reasons.

REASON 1:

Claim 1 is allowable as it recites, *inter alia*,

> wherein the motherboard enables a first and a second video card to attach, respectively, to the at least one first video card slot and second video card slot, and wherein the motherboard enables the first and the second video cards to operate in parallel to output graphics data to a single visual display device, and

> wherein said switch is configured to distribute lanes dynamically during operation including data transmission to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards. (emphasis added).

Levy fails to teach or suggest the features of independent claim 1, and in particular fails to teach "wherein said switch is configured to distribute lanes dynamically during operation including data transmission to said plurality of high-speed video card slots responsive to changes in bandwidth needs during processing by said video cards." Levy does not disclose a switch "configured to distribute lanes dynamically during operation including data transmission" and therefore does not disclose all the features of Claim 1.

Indeed, the Office Action acknowledges that Levy does not disclose this feature through stating, "the claims do not recite 'during operation' means during outputting data." (Office Action at 4). Applicant has amended Independent claim 1 to expressly recite "dynamically during operation including data transmission" to further clarify that Levy does not disclose a switch as claimed. Even more, Levy does not disclose the DEVICES[1] can be operating, -- *i.e.*, processing or outputting data -- while the switch dynamically distributes the lanes in response to changes in bandwidth needs. Unlike the present invention, Levy discloses that "the DEVICES 0-5 in other embodiments may initiate their port identification methods in response to other events such as, for example, a root reset or a request to re-identify its ports." *See* paragraph [0042] of Levy. This disclosure of initiating port identification and requests to re-identify ports is insufficient to disclose the switch of Claim as presently claimed. For at least these reasons, Applicant respectfully submits that the rejection should be withdrawn.

[1] Such as for example, Ethernet cards, video cards, RAID controllers, SCSI Controllers, ATA disk controllers, PCI bridges, etc coupled to a root device (DEVICE 0) of the chipset 104. [0016] of Levy.

REASON 2:

In addition, claim 1 is also allowable as it recites, *inter alia*,

> a switch connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots. (emphasis added).

Applicant, further respectfully directs the Office to the specification at page 27 and FIG. 8, illustrating an embodiment and disclosing,

> [t]he PCI Express switch 880 converts the sixteen lanes 871 coming from the chipset 220 root complex into two or more distributed x16 links 872, each connected to a x16 PCI Express Graphics slot.

Levy fails to teach or suggest the features of independent claim 1. The Office purports that these features are taught by Levy in stating the following,

> [s]ince the port transmitters 116 perform the port identification, this meant that the port transmitter 116 is capable of converting the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection each of said plurality of high-speed video card slots. (Office Action at 3).

Applicant respectfully traverse this assertion as an improper reliance on inherency. The reliance is improper as the alleged teachings do not necessarily flow port transmitters 116 performing port identification as required for inherency. *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (That is, "[i]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that

the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.") (emphasis in original).

More specifically, Levy discloses in paragraph [0022],

> [0022] The ports $112_1 \ldots 112_X$ may further comprise one or more decoders $181_1 \ldots 118_X$ to decode encoded data units or symbols received from its corresponding port receiver $114_1 \ldots 114_X$, and may also comprise one or more encoders $120_1 \ldots 120_X$ to generate encoded data units or symbols to be transmitted by its corresponding port transmitter $116_1 \ldots 116_X$. In another embodiment, the ports $112_1 \ldots 112_X$ may comprise one or more codecs that comprise a unified encoder/decoder instead of separate decoders $118_1 \ldots 118_X$ and encoders $120_1 \ldots 120_X$ as depicted. Further, the decoders $118_1 \ldots 118_X$ and the encoders $120_1 \ldots 120_X$ may comprise buffers to provide buffer storage for data units and symbols being transferred.

As shown from the foregoing, there is no teaching or suggestion of "a switch connected to said interconnect and adapted to convert the interconnect lanes into a plurality of distributed links such that there is a different one of said distributed links providing a connection to each of said plurality of high-speed video card slots" as recited in independent claim 1. Moreover, these features do not necessarily flow from the above disclosure. For at least these reasons, Applicant respectfully requests withdrawal of the rejection. Amended independent claims 41 and 48 are allowable for similar reasons discussed above with respect to claim 1.

CONCLUSION

In view of the foregoing, Applicants respectfully request that the Examiner consider the claims for examination on the merits. Examiner Joni Hsu is cordially invited to contact the undersigned should she have any questions about the above remarks. Timely allowance of the pending claims is requested.

In the event that an appropriate fee amount is not enclosed by check for any fees

due in connection with the filing of this Response or requisite extensions of time, please charge any deficiencies or credit any overpayments to Deposit Account No. 50-1349.

Respectfully submitted,

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By: _____
Scott J. Hawranek
Registration No. 52,411

Paul A. Roberts
Registration No. 56,990

HOGAN & HARTSON LLP
555 13th Street, N.W.
Washington, D.C. 20004
Telephone: 202-637-5600
Facsimile: 202-637-5910
email: dcptopatent@hhlaw.com
Customer No.: 24633